ABSTRACT

A clock generator (100) with a random-number generator (1) and a phase modulator (4) is disclosed for generating a frequency-jittered system clock (cl), which thus causes minimal radiated interference. Between the random-number generator (1) and the phase modulator (4), an integrator (3) is connected for integrating the random numbers (z1) provided by the random-number generator. The output of the integrator (3) controls the respective phase value (pa) in the phase modulator (4). The integrator (3) is coupled to a checking facility (7) which interferes in the random numbers (z1, z2) and intervenes in the integration process so that predetermined limit values (G1, G1'; G2, G2'; G3, G3') are not exceeded during the integration.